UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/862,446	05/23/2001	Gregory M. Evans	EVANS 7	8876

1444 7590 02/24/2005

BROWDY AND NEIMARK, P.L.L.C.
624 NINTH STREET, NW
SUITE 300
WASHINGTON, DC 20001-5303

EXAMINER	
PHAN, TRI H	

ART UNIT	PAPER NUMBER
2661	

DATE MAILED: 02/24/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/862,446	EVANS, GREGORY M.	
	Examiner	Art Unit	
	Tri H. Phan	2661	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 May 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-40* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7,9-18 and 20-40* is/are rejected.

7)☐ Claim(s) *8 and 19* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *23 May 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☒ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *1-4*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-7, 9-18 and 20-40 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Chiu et al.** (U.S.6,597,689).

- In regard to claims 1 and 31, **Chiu** discloses in Figs. 1, 3, 5-8, 10 and 13 and in the respective portions of the specification about the *interface device and method* ('NEBS-compliant chassis' in Fig. 3 of the Intelligent Multiservice Access System 'IMAS' in Fig. 1) *for providing the gateway function between lines of the public switched telephone network 'PSTN' that carry digital hierarchy signals in a plurality of digital hierarchies and an asynchronous transfer mode 'ATM' backbone network that carries signals in ATM format* (For example see Fig. 1; col. 14, lines 18-53; col. 19, lines 38-44); *where the interface device comprises the telephony transceiver* ('xDSL modems' of the line card LIU in Fig. 8) *operative to receive upstream digital hierarchy signals in a plurality of digital hierarchies from PSTN* (For example see Figs. 5, 8; col. 23, lines 33-43; col. 32, lines 29-36; **Chiu** fails to explicitly disclose about receiving "*digital hierarchy signals from PSTN*"; however, **Chiu** does disclose wherein other loop technologies besides the

xDSL technology family such as DS3, OC-3C, OC-12C can be used through the multiple shelves interfaces as disclosed in col. 19, lines 38-44. Therefore, it would have been obvious to the person of ordinary skill in the art at the time of the invention was made to implement the multiple shelves interfaces for using "*digital hierarchy signals*" such as DS3, OC-3C, OC-12C into PSTN, with the motivation being to provide the ability for supporting multiple loop technologies), *the hierarchy converter* ('UTOPIA multiplexer/demultiplexer' in Fig. 8) *operatively associated with the telephony transceiver and operative to convert the upstream digital hierarchy signals in the plurality of digital hierarchies to upstream signals in the single digital hierarchy distributed over a plurality of logical channels* (For example see Fig. 8; col. 30, line 52 through col. 31, line 22; wherein the converting between digital hierarchy signals such as OC-3 to STS-3 is disclosed in col. 23, line 52 through col. 24, line 10), *the inverse multiplexing unit* ('framer' in the chassis switch card in Fig. 6) *operatively associated with the hierarchy converter and operative to inverse-multiplex the upstream signals in the single digital hierarchy distributed over the plurality of logical channels thereby to form upstream inverse-multiplexed digital hierarchy signals* (For example see Fig. 6-7; col. 27, lines 4-13, 53-60), *the ATM framer* ('ATM SAR' in the CPU subsystem in Figs. 6-7) *operatively associated with the inverse multiplexing unit and operative to map the upstream inverse-multiplexed digital hierarchy signals into ATM cells thereby to form upstream signals in ATM format* (For example see Fig. 6-7; col. 28, lines 34-50) *and the ATM transceiver* ('transceiver' in the uplink module in Fig. 6) *operatively associated with the ATM framer and operative to transmit the upstream signals in ATM format to the ATM backbone network* (For example see Figs. 5-6; col. 27, lines 45-52; col. 21, lines 14-29).

- Regarding to claims 2-3, 13-14 and 34, **Chiu** further discloses about the transceivers and framer ("*telephony transceiver*") with different interfaces for supporting the OC-3, DS-3, T3, and E3 ("*digital hierarchy signals*"; For example see Fig. 6; col. 27, lines 53-60; col. 29, lines 11-15).

- In regard to claims 4 and 15, **Chiu** further discloses about the UTOPIA mux/demux ("*hierarchy converter*"; For example see Fig. 8; col. 30, line 52 through col. 31, line 22).

- Regarding claims 5 and 16, **Chiu** further discloses about the framers in the chassis switch card for performing the multiplexing function, e.g. aggregating ATM cells from the line cards into one of the telecommunications backbone-side links ("*inverse multiplexers*"; For example see Fig. 6; col. 27, lines 4-13).

- In regard to claims 6-7 and 17-18, **Chiu** further discloses about the transceiver ("*ATM transceiver*"; For example see Fig. 6; col. 27, lines 45-60) and the bus 94 ("*ATM bus*") for handling the ATM cells with UTOPIA interface between the telecommunications backbone-side through the framer ("*inverse multiplexing unit*") and the LIU-side line cards through the ATM SAR ("*ATM framer*") in the CPU subsystem (For example see Fig. 6; col. 27, lines 1-44).

- Regarding claims 9, 20, 37 and 39, **Chiu** further discloses about the ATM SAR using AAL5 for supporting CBR, VBR, ABR, and UBR traffic classes ("*CBR*"; For example see col.

28, lines 45-50; wherein the CBR is used for types of data where end systems require time synchronization and response time, e.g. "*time relation between endpoints of connections*", as disclosed in col. 5, lines 20-27), but fails to explicitly disclose about "*AAL1*". However, the ATM Adaption Layer or AAL is software application which use to adapt or convert the different application data unit sizes relying on different application requirements into ATM cell format (For example see col. 63, lines 36-49). Thus, it would have been obvious to the person of ordinary skill in the art at the time of the invention was made to combine the "*AAL1*" into the AAL software application of the **Chiu**'s ATM SAR, with the motivation being to improve the ability to convert different application data unit sizes with different requirements of AAL types, such as "*AAL1*".

- In regard to claims 10, 21, 38 and 40, **Chiu** further discloses about the Frame relay/ATM (For example see Fig. 1). Thus, **Chiu** fails to explicitly disclose about the Frame-Relay/ATM internetworking "*circuitry*" in the IMAS device; however, it would have been obvious to the person of ordinary skill in the art at the time of the invention was made to combine the Frame-Relay/ATM internetworking "*circuitry*" in the other interface technologies of the IMAS device, with the motivation being to provide services for Frame Relay disclosed in Fig. 1.

- Regarding claim 11, **Chiu** further discloses about the S/UNI (For example see Fig. 7; col. 29, lines 11-15), which receives the OC-3 signals ("*digital hierarchy signals*") from the telecommunications backbone-side and transmits to the ATM SAR ("*ATM framer*") via the bus

for segmenting and reassembling data into ATM cells ("*mapping and forming digital hierarchy signals into ATM cells*"; For example see Figs. 6-7; col. 28, lines 34-50).

- In regard to claims 12 and 32-33, **Chiu** discloses in Figs. 1, 3, 5-8, 10 and 13 and in the respective portions of the specification about the *interface device and method* ('NEBS-compliant chassis' in Fig. 3 of the Intelligent Multiservice Access System 'IMAS' in Fig. 1) *for providing the gateway function between lines of the public switched telephone network 'PSTN' that carry digital hierarchy signals in a plurality of digital hierarchies and an asynchronous transfer mode 'ATM' backbone network that carries signals in ATM format* (For example see Fig. 1; col. 14, lines 18-53; col. 19, lines 38-44); *where the interface device comprises the ATM transceiver* ('transceiver' in Fig. 6) *operative to receive the downstream signals in ATM format from the ATM backbone network* (For example see Figs. 5-6; col. 27, lines 45-52; col. 21, lines 14-29), *the ATM UTOPIA framer* ('ATM SAR' in the CPU subsystem in Figs. 6-7) *operatively associated with the ATM transceiver and operative to map the downstream signals in ATM format into downstream digital hierarchy signals* (For example see Fig. 6-7; col. 28, lines 34-50; Fig. 10; col. 44, lines 46-53; and where "*downstream*" is the opposite direction with the "*upstream*" disclosed above; and wherein the ATM SAR provide reassembly functionality to convert cells into frames and sends to the framer via the bus for transmitting to the telecommunications backbone-side OC-3c lines or DS3, T3, and E3 "*digital hierarchy signals*" as disclosed in col. 27, lines 53-60; col. 29, lines 11-15), *the inverse multiplexing unit* ('framer' in the chassis switch card in Fig. 6) *operatively associated with the ATM framer and operative to inverse-demultiplex the downstream digital hierarchy signals for providing downstream signals in the single digital*

hierarchy distributed over the plurality of logical channels (For example see Fig. 6-7; col. 27, lines 53-60), *the hierarchy converter* ('UTOPIA multiplexer/demultiplexer' in Fig. 8) *operatively associated with the inverse multiplexing unit and operative to convert the downstream signals in the single digital hierarchy distributed over a plurality of logical channels* (For example see Fig. 8; col. 30, line 52 through col. 31, line 22; wherein the converting between digital hierarchy signals such as OC-3 to STS-3 is disclosed in col. 23, line 52 through col. 24, line 10), *the telephony transceiver* ('xDSL modems' of the line card LIU in Fig. 8) *operatively associated with the hierarchy converter and operative to transmit downstream digital hierarchy signals in a plurality of digital hierarchies from PSTN* (For example see Figs. 5, 8; col. 23, lines 33-43; col. 32, lines 29-36). **Chiu** fails to explicitly disclose about transmitting downstream "*digital hierarchy signals to the PSTN*"; however, **Chiu** does disclose wherein other loop technologies besides the xDSL technology family such as DS3, OC-3C, OC-12C can be used through the multiple shelves interfaces as disclosed in col. 19, lines 38-44.

Therefore, it would have been obvious to the person of ordinary skill in the art at the time of the invention was made to implement the multiple shelves interfaces for using "*digital hierarchy signals*" such as DS3, OC-3C, OC-12C into PSTN, with the motivation being to provide the ability for supporting multiple loop technologies.

- Regarding claims 22-23, **Chiu** further discloses about the Intelligent Multiservice Access System 'IMAS' ("*communication device*"; For example see Fig. 1; col. 20, lines 50-62)

comprising the NEBS-compliant chassis ("*interface device*" of claim 1 and claim 12; For example see Fig. 3).

- In regard to claims 24-25, **Chiu** further discloses about the Intelligent Multiservice Access System 'IMAS' at the central office; which comprises the NEBS-compliant chassis ("*interface device*" of claim 1 and claim 12; For example see Fig. 3) for working in the telecommunications network from the subscribers to the telecommunications backbone ("*communication network comprising PSTN and ATM backbone network*"; For example see Fig. 1; col. 14, line 20 through col. 15, line 67).

- In regard to claims 29-30, **Chiu** further discloses about the ATM switch core/fabric in the IMAS ("*ATM switch fabric*"; For example see col. 19, lines 61-64; col. 54, lines 10-17; col. 60, lines 35-54).

- Regarding claims 35-36, **Chiu** further discloses about the *inverse multiplexing unit* ('framer' in the chassis switch card in Fig. 6; 'S/UNI' in Fig. 7; which uses to mux/demux the OC-3 signals) *operatively associated with the ATM framer and operative to inverse-demultiplex the downstream digital hierarchy signals for providing downstream signals in the single digital hierarchy distributed over the plurality of logical channels* (For example see Fig. 6-7; col. 27, lines 53-60; col. 29, lines 11-15).

3. Claims 26-28 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Chiu et al.** (U.S.6,597,689) as applied to claims 1 and 12 above, and further in view of **Swerdlow** (U.S.5,995,504).

- In regard to claims 26-28, **Chiu** discloses in Figs. 1, 3, 5-8, 10 and 13 and in the respective portions of the specification about the *interface device and method* ('NEBS-compliant chassis' in Fig. 3 of the Intelligent Multiservice Access System 'IMAS' in Fig. 1) *for providing the gateway function between lines of the public switched telephone network 'PSTN' that carry digital hierarchy signals in a plurality of digital hierarchies and an asynchronous transfer mode 'ATM' backbone network that carries signals in ATM format* (For example see Fig. 1; col. 14, lines 18-53; col. 19, lines 38-44); *where the interface device comprises the telephony transceiver* ('xDSL modems' of the line card LIU in Fig. 8) *operative to receive upstream digital hierarchy signals in a plurality of digital hierarchies from PSTN* (For example see Figs. 5, 8; col. 23, lines 33-43; col. 32, lines 29-36; **Chiu** fails to explicitly disclose about receiving "*digital hierarchy signals from PSTN*"; however, **Chiu** does disclose wherein other loop technologies besides the xDSL technology family such as DS3, OC-3C, OC-12C can be used through the multiple shelves interfaces as disclosed in col. 19, lines 38-44. Therefore, it would have been obvious to the person of ordinary skill in the art at the time of the invention was made to implement the multiple shelves interfaces for using "*digital hierarchy signals*" such as DS3, OC-3C, OC-12C into PSTN, with the motivation being to provide the ability for supporting multiple loop technologies), *the hierarchy converter* ('UTOPIA multiplexer/demultiplexer' in Fig. 8) *operatively associated with the telephony transceiver and operative to convert the upstream*

digital hierarchy signals in the plurality of digital hierarchies to upstream signals in the single digital hierarchy distributed over a plurality of logical channels (For example see Fig. 8; col. 30, line 52 through col. 31, line 22; wherein the converting between digital hierarchy signals such as OC-3 to STS-3 is disclosed in col. 23, line 52 through col. 24, line 10), *the inverse multiplexing unit* ('framer' in the chassis switch card in Fig. 6) *operatively associated with the hierarchy converter and operative to inverse-multiplex the upstream signals in the single digital hierarchy distributed over the plurality of logical channels thereby to form upstream inverse-multiplexed digital hierarchy signals* (For example see Fig. 6-7; col. 27, lines 4-13, 53-60), *the ATM framer* ('ATM SAR' in the CPU subsystem in Figs. 6-7) *operatively associated with the inverse multiplexing unit and operative to map the upstream inverse-multiplexed digital hierarchy signals into ATM cells thereby to form upstream signals in ATM format* (For example see Fig. 6-7; col. 28, lines 34-50) *and the ATM transceiver* ('transceiver' in the uplink module in Fig. 6) *operatively associated with the ATM framer and operative to transmit the upstream signals in ATM format to the ATM backbone network* (For example see Figs. 5-6; col. 27, lines 45-52; col. 21, lines 14-29). Thus, **Chiu** does disclose about the PSTN with the DS3/OC3/ATM communication line, but fails to explicitly disclose about the "*DACS*". However, such implementation is known in the art.

For example, **Swerdlow** discloses about the system and method for controlling multiplexers and cross-connects on the telecommunications network (For example see Figs. 2, 9-10; Abstract); wherein the cross-connect machines DCS 3/1, DCS 1/0 interchange the bit rate channels ("*DACS*"; For example see Figs. 2, 9; col. 1, lines 41-57; col. 3, lines 41-46) and the SONET Mux OC-48, OC-3 multiplexe the DS signals into STS signals at the feeder and

breakout sites ("SONET multiplexer"; For example see Fig. 2; col. 2, lines 4-46; col. 3, lines 47-67).

Thus it would have been obvious to the person of ordinary skill in the art at the time of the invention was made to implement the invention as taught by **Swerdlow** into the **Chiu**'s system, with the motivation being to improve the ability to control multiplexers and cross-connects by interchanging between different bit rates and mux the signals into OC signals for transmitting over in the telecommunications network disclosed in **Chiu**: col. 2, lines 48-63.

Reasons For Allowance

4. Claims 8 and 19 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter: Many references in the art disclose the system and method for transmission ATM/packet over SONET/SDH. Most of those references are comprising the telephony transceiver, the hierarchy converter, the inverse multiplexing unit, the ATM framer and the ATM transceiver; wherein the ATM cells are transmitted over the ATM bus between the inverse multiplexing unit and the ATM framer, such as that found in **Chiu et al.** (U.S.6,597,689), **Lewis et al.** (U.S.6,005,865), **Parruck et al.** (U.S.6,751,224). But no prior art reference utilizes the ATM UTOPIA framer and the multi-UTOPIA bus.

Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Parruck et al. (U.S.6,751,224), **Yu, Shaohua** (U.S.2001/0012288), **Lewis et al.** (U.S.6,005,865), **Park et al.**, (Implementation of the ATM Adaption Layer for VTOA services, ICICS, Singapore, 9-12 Sept 1997, IEEE, 0-7803-3676-3/97, 1997, pages 786-789), **Sunaga et al.**, (System Architecture for a Large-Scale Public VTOA Handling Node, NTT Network Service System Laboratories, IEEE, 0-7803-4788-9/98, 1998, pages 275-280) and **Grilo et al.**, (VTOA/VoIP/ISDN Telephone Gateway, INESC, Portugal, IEEE, 0-7803-5428-1/99, 1999, pages 230-235) are all cited to show devices and methods for improving modem communication architectures, which are considered pertinent to the claimed invention.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tri H. Phan, whose telephone number is (571) 272-3074. The examiner can normally be reached on M-F (8:00-4:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chau T. Nguyen can be reached on (571) 272-3126.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks
Washington, D.C. 20231

or faxed to:

(703) 872-9314

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA, Sixth Floor.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Technology Center 2600 Customer Service Office, whose telephone number is (703) 305-3900.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

BRIAN NGUYEN
PRIMARY EXAMINER

Tri H. Phan
February 18, 2005